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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,235	06/29/1999	YASUHIKO TAKEMURA	0756-1980ELE	6257

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EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

BL

Office Action Summary	Application No.	Applicant(s)	
	09/342,235	TAKEMURA, YASUHIKO	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/30/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed March 30, 2006 has been entered; no new claims have been introduced.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. ("Yamazaki") USPN 5,905,555 in view of Takahata ("Takahata") JP 63-076474 (of record).

Yamazaki discloses (fig. 8 and col. 10, lines 35-45) a semiconductor device comprising a substrate having an insulating surface; at least first and second semiconductor islands comprising polysilicon (as in claim 8) formed over said substrate wherein each of the semiconductor islands has a channel region 28/28'and a pair of impurity regions 34a/34b, 34a'/34b'; an insulating film 35 formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively; at least first and second gate electrodes 40/40' formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring 36b' being connected to said one of the impurity regions through a hole 39 opened in said insulating film; a data line 36a' formed on said insulating film connected to the other one of

the impurity regions of the first semiconductor island; a first interlayer insulating film 37 (fig. 8E) formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line; a voltage supply line 36b formed on said first interlayer insulating film connected to one of the pair of impurity regions of the second semiconductor island; a second interlayer insulating film 39 (fig. 8F) or a surface smoothing film 39 (as in claim10) formed over said first interlayer insulating film and said voltage supply line; a pixel electrode 37 comprising an ITO (as in claim 7) formed over said second interlayer insulating film connected to the other one of the pair of the impurity regions of the second semiconductor island, but lacks anticipation of a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode .

Takahata discloses in figs. 2 and 6 a semiconductor device comprising a substrate 1 having an insulating surface; at least first and second semiconductor islands 2 comprising polysilicon (as in claim 8) formed over said substrate, wherein each of the semiconductor islands has a channel region and a pair of impurity regions 5; a first and a second gate insulating film 3 formed over said semiconductor island, respectively; at least first and second gate electrodes 4 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; **a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode (fig. 2);** an interlayer insulating film 3 formed over said wiring.

Therefore, in view of Takahata's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki's device by incorporating Takahata teachings since that would enhance speed as taught by Takahata.

4. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Takahata.

Yamazaki discloses (fig. 8 and col. 10, lines 35-45) a semiconductor device comprising a substrate having an insulating surface; at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region 28/28'and a pair of impurity regions 34a/34b, 34a'/34b'; an insulating film 35 formed over said substrate, said insulating film including at least first and second gate insulating films formed over said first and second semiconductor islands, respectively; at least first and second gate electrodes 40/40' formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring 36b' being connected to said one of the impurity regions through a hole 39 opened in said insulating film; a data line 36a' formed on said insulating film connected to the other one of the impurity regions of the first semiconductor island; a first interlayer insulating film 37 (fig. 8E) formed over the first and second semiconductor islands, the first and second gate electrodes, the wiring and the data line; a voltage supply line 36b formed on said first interlayer insulating film connected to one of the pair of impurity regions of the second semiconductor island; an address line (not shown in fig. 8 but is conventional for address line to extend across a data line); a second interlayer insulating film or a surface smoothing layer 39 (as in claim 11) (fig. 8F) formed over said first interlayer insulating film and said voltage supply line; a pixel electrode 37 formed over said second interlayer insulating film connected to the other one of the pair of the impurity regions of the second semiconductor island, but lacks anticipation of a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode .

Takahata discloses in figs. 2 and 6 a semiconductor device comprising a substrate 1 having an insulating surface; at least first and second semiconductor islands 2 formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions 5; a first and a second gate insulating film 3 formed over said semiconductor island, respectively; at least first and second gate electrodes 4 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; **a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode (fig. 2);** an interlayer insulating film 3 formed over said wiring.

Therefore, in view of Takahata's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki's device by incorporating Takahata teachings since that would enhance speed as taught by Takahata.

Response to Arguments

5. Applicant's arguments filed 3/30/2006 have been fully considered but they are not persuasive.

6. Applicants argue that there in no motivation or suggestion to combine the references of Yamazaki and Takahata.

7. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, what is not taught by Yamazaki, namely **a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode** is clearly disclosed by Takahata. Since Yamazaki does not teach away from such modification, a person skilled in the art would have found the motivation to connect one of the impurity regions of the first semiconductor island with the second gate electrode so as to enhance speed as taught by Takahata.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Unagami et al. (USPN 4,528,480) disclose in fig. 1 a semiconductor device including an address line 22 connected to a gate electrode 36a, wherein said address line extends across a data line 20.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ANS
June 6, 2006